Claims

We Claim:

1. A method of designing an electrical wiring structure having a plurality of wires, said method comprising identifying at least one wire pair, said wire pair including a first wire of the plurality of wires and a second wire of the plurality of wires, said second wire already tri-stated or can be tri-stated, said wire pair having a same-direction switching probability ϕ_{SD} per clock cycle that is no less than a pre-selected minimum same-direction switching probability $\phi_{SD,MIN}$ or having an opposite-direction switching probability ϕ_{OD} per clock cycle that is no less than a pre-selected minimum opposite-direction switching probability $\phi_{OD,MIN}$, said first wire and said second wire satisfying at least one mathematical relationship, said at least one mathematical relationship involving L_{COMMON} and $W_{SPACING}$, said $W_{SPACING}$ defined as a spacing between the first wire and the second wire, said L_{COMMON} defined as a common run length of the first wire and the second wire.

2. The method of claim 1, said at least one mathematical relationship comprising:

$W_{SPACING}$ no greater than a pre-selected minimum spacing $W_{SPACING, MAX}$; and

L_{COMMON} no less than a pre-selected minimum common run length $L_{COMMON, MIN}$.

3. The method of claim 1, said at least one mathematical relationship comprising $F_{LW} \geq F_{LW,MIN}$, said F_{LW} defined as $L_{COMMON}/W_{SPACING}$, said $F_{LW,MIN}$ defined as a pre-selected minimum value of F_{LW}.

4. The method of claim 1, wherein identifying at least one wire pair comprises:

identifying at least one high-power wire; and

for a high-power wire of the at least one high-power wire, identifying a good neighbor wire of the high-power wire, wherein the first wire of the wire pair is the high-power wire, and wherein the second wire of the wire pair is the good neighbor wire.

5. The method of claim 1, wherein said second wire is not already tri-stated but can be tri-stated, and further comprising adding tri-stating logic to the second wire.

6. The method of claim 1, wherein ϕ_{OD} is no less than $\phi_{OD,MIN}$, and further comprising adding logic for inverting the second wire along the common run length.

7. The method of claim 1, further comprising adding blocking logic for blocking propagation of a signal from the second wire while the second wire is tri-stated.

8. The method of claim 1, further comprising reducing $W_{SPACING}$.

9. The method of claim 1, wherein the at least one wire pair includes a plurality of wire pairs, and further comprising:

ranking the wire pairs in accordance with power dissipation savings;

developing a list of the ranked wire pairs in sorted order of the power dissipation savings; and

truncating the list at a point of diminishing returns in the power dissipation savings, in accordance with a predetermined truncation criterion.

10. The method of claim 1, wherein $W_{SPACING}$ is a predetermined spacing, and wherein L_{COMMON} is a predetermined common run length.

11. The method of claim 1, wherein $W_{SPACING}$ is an established spacing, and wherein L_{COMMON} is an established common run length.

12. A method for executing a two-wire voltage transition, comprising the steps of:

providing two wires of an electrical wire network, said two wires denoted as an A wire and a B wire, said A wire having a capacitance C_A, said B wire having a capacitance C_B, said A wire and B wire having a coupling capacitance C_C between the A wire and the B wire;

tri-stating the B wire from a voltage V_{B1} to a high impedance state;

after tri-stating the B wire, transitioning the A wire from a voltage V_{A1} to a voltage V_{A2} such that $V_{A2} \neq V_{A1}$; and

after transitioning the A wire to V_{A2}, transitioning the B wire to a voltage V_{B2} such that $V_{B2} \neq V_{B1}$.

13. The method of claim 12, wherein $(V_{A2} - V_{A1})(V_{B2} - V_{B1}) > 0$.

14. The method of claim 13, wherein the A wire and the B wire have a same-direction switching probability per clock cycle ϕ_{SD} that is no less than a pre-selected minimum same-direction switching probability $\phi_{SD,MIN}$.

15. The method of claim 13, wherein $V_{A1} = V_{B1} = 0$ and $V_{A2} = V_{B2} = 1$, and wherein an effective capacitance of the two-wire voltage transition is $C_A + C_B$.

16. The method of claim 13, wherein $V_{A1} = V_{B1} = 1$ and $V_{A2} = V_{B2} = 0$, and wherein an effective capacitance of the two-wire voltage transition is 0.

17. The method of claim 12, wherein $(V_{B2} - V_{B1})(V_{A2} - V_{A1}) < 0$, wherein the A wire and the B wire have a common run length, and further comprising inverting the B wire along the common run length.

18. The method of claim 17, wherein the A wire and the B wire have an opposite-direction switching probability per clock cycle ϕ_{OD} that is no less than a pre-selected minimum opposite-direction switching probability $\phi_{OD,MIN}$.

19. The method of claim 17, wherein $V_{A1} = 0$, $V_{B1} = 1$, $V_{A2} = 1$, and $V_{B2} = 0$, and wherein an effective capacitance of the two-wire voltage transition is $C_A + C_B$.

20. The method of claim 17, wherein $V_{A1} = 1$, $V_{B1} = 0$, $V_{A2} = 0$, and $V_{B2} = 1$, and wherein an effective capacitance of the two-wire voltage transition is 0.

21. The method of claim 12, further comprising blocking propagation of a signal from the B wire while the B wire is tri-stated.

22. An electrical wiring structure, comprising at least one wire pair, said wire pair including a first wire and a second wire, said second wire slated for being tri-stated, said wire pair having a same-direction switching probability ϕ_{SD} per clock cycle that is no less than a pre-selected minimum same-direction switching probability $\phi_{SD,MIN}$ or having an opposite-direction switching probability ϕ_{OD} per clock cycle that is no less than a pre-selected minimum opposite-direction switching probability $\phi_{OD,MIN}$, said first wire and said second wire satisfying at least one mathematical relationship, said at least one mathematical relationship involving L_{COMMON} and $W_{SPACING,}$ said $W_{SPACING}$ defined as a spacing between the first wire and the second wire, said L_{COMMON} defined as a common run length of the first wire and the second wire.

23. The electrical wiring design of claim 22, said at least one mathematical relationship comprising:

$W_{SPACING}$ no greater than a pre-selected minimum spacing $W_{SPACING,\,MAX}$; and

L_{COMMON} no less than a pre-selected minimum common run length $L_{COMMON,\,MIN}$.

24. The electrical wiring design of claim 22, said at least one mathematical relationship comprising $F_{LW} \geq F_{LW,MIN}$, said F_{LW} defined as $L_{COMMON}/W_{SPACING}$, said $F_{LW,MIN}$ defined as a pre-selected minimum value of F_{LW}.

25. The electrical wiring design of claim 22, wherein the first wire of the wire pair is a high-power wire, and wherein the second wire of the wire pair is a good neighbor wire of the high

power wire.

26. The electrical wiring design of claim 22, wherein ϕ_{OD} is no less than $\phi_{OD,MIN}$, and further comprising logic for inverting the second wire along the common run length.

27. The electrical wiring design of claim 22, further comprising blocking logic for blocking propagation of a signal from the second wire while the second wire is tri-stated.

28. The electrical wiring design of claim 22, wherein $W_{SPACING}$ is a predetermined spacing, and wherein L_{COMMON} is a predetermined common run length.

29. The electrical wiring design of claim 22, wherein $W_{SPACING}$ is an established spacing, and wherein L_{COMMON} is an established common run length.

30. An electrical wire structure, comprising two wires of a wire network, said two wires denoted as an A wire and a B wire, said A wire having a capacitance C_A, said B wire having a capacitance C_B, said A wire and B wire having a coupling capacitance C_C between the A wire and the B wire, said B wire in a tri-state, said A wire transitioning from a voltage V_{A1} to a voltage V_{A2} such that $V_{A2} \neq V_{A1}$, said B wire having transitioned to the tri-state from a voltage V_{B1}, said B wire intended to be transitioned to a voltage V_{B2} such that $V_{B2} \neq V_{B1}$ after the A wire has transitioned to the voltage V_{A2}, said transition of the A wire from the voltage V_{A1} to the voltage V_{A2} and of the B wire from the voltage V_{B1} to the voltage V_{B2} identified as a two-wire voltage transition.

31. The electrical wire network of claim 30, wherein $(V_{A2}-V_{A1})(V_{B2}-V_{B1}) > 0$.

32. The electrical wire network of claim 31, wherein the A wire and the B wire have a same-direction switching probability per clock cycle ϕ_{SD} that is no less than a pre-selected minimum same-direction switching probability $\phi_{SD,MIN}$.

33. The electrical wire network of claim 31, wherein $V_{A1} = V_{B1} = 0$ and $V_{A2} = V_{B2} = 1$, and wherein an effective capacitance of the two-wire voltage transition is $C_A + C_B$.

34. The electrical wire network of claim 31, wherein $V_{A1} = V_{B1} = 1$ and $V_{A2} = V_{B2} = 0$, and wherein an effective capacitance of the two-wire voltage transition is 0.

35. The electrical wire network of claim 30, wherein $(V_{B2} - V_{B1})(V_{A2} - V_{A1}) < 0$, wherein the A wire and the B wire have a common run length, and further comprising the B wire inverted along the common run length.

36. The electrical wire network of claim 35, wherein the A wire and the B wire have an opposite-direction switching probability per clock cycle ϕ_{OD} that is no less than a pre-selected minimum opposite-direction switching probability $\phi_{OD,MIN}$.

37. The electrical wire network of claim 35, wherein $V_{A1} = 0$, $V_{B1} = 1$, $V_{A2} = 1$, and $V_{B2} = 0$, and wherein an effective capacitance of the two-wire voltage transition is $C_A + C_B$.

38. The electrical wire network of claim 35, wherein $V_{A1} = 1$, $V_{B1} = 0$, $V_{A2} = 0$, and $V_{B2} = 1$, and wherein an effective capacitance of the two-wire voltage transition is 0.

39. The electrical wire network of claim 30, wherein propagation of a signal from the B wire while the B wire is being blocked.

40. A computer system for designing an electrical wiring structure having a plurality of wires, comprising:

a processor;

an input device coupled to the processor;

an output device coupled to the processor;

a first memory device coupled to the processor;

a second memory device coupled to the processor;

a computer code stored in the second memory device and executed by the processor; said computer code comprising an algorithm, said algorithm identifying at least one wire pair, said wire pair including a first wire of the plurality of wires and a second wire of the plurality of wires, said second wire already tri-stated or can be tri-stated, said wire pair having a same-direction switching probability ϕ_{SD} per clock cycle that is no less than a pre-selected minimum same-direction switching probability $\phi_{SD,MIN}$ or having an opposite-direction switching probability ϕ_{OD} per clock cycle that is no less than a pre-selected minimum opposite-direction switching probability $\phi_{OD,MIN}$, said first wire and said second wire satisfying at least one mathematical relationship, said at least one mathematical relationship involving L_{COMMON} and $W_{SPACING}$, said $W_{SPACING}$ defined as a spacing between the first wire and the second wire, said L_{COMMON} defined as a common run length of the first wire and the second wire.

41. The computer system of claim 40, said at least one mathematical relationship comprising:

$W_{SPACING}$ no greater than a pre-selected minimum spacing $W_{SPACING. MAX}$; and

L_{COMMON} no less than a pre-selected minimum common run length $L_{COMMON, MIN}$.

42. The computer system of claim 40, said at least one mathematical relationship comprising $F_{LW} \geq F_{LW,MIN}$, said F_{LW} defined as $L_{COMMON}/W_{SPACING}$, said $F_{LW,MIN}$ defined as a pre-selected minimum value of F_{LW}.

43. The computer system of claim 40, wherein said algorithm identifying at least one wire pair includes:

said algorithm identifying at least one high-power wire; and

for a high-power wire of the at least one high-power wire, said algorithm identifying a good neighbor wire of the high-power wire, wherein the first wire of the wire pair is the high-power wire, and wherein the second wire of the wire pair is the good neighbor wire.

44. The computer system of claim 40, wherein if said algorithm determines that said second wire is not already tri-stated but can be tri-stated, then further comprising said algorithm adding tri-stating logic to the second wire.

45. The computer system of claim 40, wherein if said algorithm determines that ϕ_{OD} is no less than $\phi_{OD,MIN}$, then further comprising said algorithm adding logic for inverting the second wire along the common run length.

46. The computer system of claim 40, further comprising the computer algorithm adding blocking logic for blocking propagation of a signal from the second wire while the second wire is tri-stated.

47. The computer system of claim 40, further comprising the computer algorithm reducing $W_{SPACING}$.

48. The computer system of claim 40, wherein if said the computer algorithm identifies the at least one wire pair as including a plurality of wire pairs, then further comprising:

said computer algorithm ranking the wire pairs in accordance with power dissipation savings;

said computer algorithm developing a list of the ranked wire pairs in sorted order of the power dissipation savings; and

said computer algorithm truncating the list at a point of diminishing returns in the power dissipation savings, in accordance with a predetermined truncation criterion.

49. The computer system of claim 40, wherein $W_{SPACING}$ is a predetermined spacing, and wherein L_{COMMON} is a predetermined common run length.

50. The computer system of claim 40, wherein $W_{SPACING}$ is an established spacing, and wherein L_{COMMON} is an established common run length.

51. A computer program product, comprising: a computer usable medium having a computer readable program code embodied therein for designing an electrical wiring structure having a plurality of wires, wherein the computer readable program code includes an algorithm, said algorithm identifying at least one wire pair, said wire pair including a first wire of the plurality of wires and a second wire of the plurality of wires, said second wire already tri-stated or can be tri-stated, said wire pair having a same-direction switching probability ϕ_{SD} per clock cycle that is no less than a pre-selected minimum same-direction switching probability $\phi_{SD,MIN}$ or having an opposite-direction switching probability ϕ_{OD} per clock cycle that is no less than a pre-selected minimum opposite-direction switching probability $\phi_{OD,MIN}$, said first wire and said second wire satisfying at least one mathematical relationship, said at least one mathematical relationship involving L_{COMMON} and $W_{SPACING}$, said $W_{SPACING}$ defined as a spacing between the first wire and the second wire, said L_{COMMON} defined as a common run length of the first wire and the second wire.

52. The computer program product of claim 51, said at least one mathematical relationship comprising:

$W_{SPACING}$ no greater than a pre-selected minimum spacing $W_{SPACING, MAX}$; and

L_{COMMON} no less than a pre-selected minimum common run length $L_{COMMON, MIN}$.

53. The computer program product of claim 51, said at least one mathematical relationship comprising $F_{LW} \geq F_{LW.MIN}$, said F_{LW} defined as $L_{COMMON}/W_{SPACING}$, said $F_{LW,MIN}$ defined as a pre-

selected minimum value of F_{LW}.

54. The computer program product of claim 51, wherein said algorithm identifying at least one wire pair includes:

said algorithm identifying at least one high-power wire; and

for a high-power wire of the at least one high-power wire, said algorithm identifying a good neighbor wire of the high-power wire, wherein the first wire of the wire pair is the high-power wire, and wherein the second wire of the wire pair is the good neighbor wire.

55. The computer program product of claim 51, wherein if said algorithm determines that said second wire is not already tri-stated but can be tri-stated, then further comprising said algorithm adding tri-stating logic to the second wire.

56. The computer program product of claim 51, wherein if said algorithm determines that ϕ_{OD} is no less than $\phi_{OD,MIN}$, then further comprising said algorithm adding logic for inverting the second wire along the common run length.

57. The computer program product of claim 51, further comprising the computer algorithm adding blocking logic for blocking propagation of a signal from the second wire while the second wire is tri-stated.

58. The computer program product of claim 51, further comprising the computer algorithm reducing $W_{SPACING}$.

59. The computer program product of claim 51, wherein if said the computer algorithm identifies the at least one wire pair as including a plurality of wire pairs, then further comprising:

said computer algorithm ranking the wire pairs in accordance with power dissipation savings;

said computer algorithm developing a list of the ranked wire pairs in sorted order of the power dissipation savings; and

said computer algorithm truncating the list at a point of diminishing returns in the power dissipation savings, in accordance with a predetermined truncation criterion.

60. The computer program product of claim 51, wherein $W_{SPACING}$ is a predetermined spacing, and wherein L_{COMMON} is a predetermined common run length.

61. The computer program product of claim 51, wherein $W_{SPACING}$ is an established spacing, and wherein L_{COMMON} is an established common run length.